A GaAs MMIC PIN DIODE RECEIVER PROTECTOR WITH SWITCHABLE ATTENUATOR

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ABSTRACT

Design and performance of a unique X-band GaAs MMIC PIN diode receiver protector (RP) with switchable attenuator is described with a maximum average and peak leakage levels of 17 dBm and 20 dBm respectively. The fast acting 8 diode RP requires no external biasing and exhibits a recovery time of 50 ns. The MMIC includes a switchable 13 dB attenuator after the RP. Two RP/Attenuator circuits for balanced operation are included in a 120 by 150 by 6 mil MMIC which exhibits only 0.55 to 0.7 dB loss, and a return loss of 15 to 30 dB over an octave bandwidth.

INTRODUCTION

In the past high power receiver protectors and attenuators were implemented using PIN diodes in packages or in chip form. The package designs have limited bandwidth at X-band and above [1] and the broadband PIN diode chip design requires specialized assembly manufacturing processes. Recently MMIC PIN diode limiters have been developed [2,3] which overcome the deficiencies of the discrete designs but have moderate power handling capability.

A PIN diode MMIC receiver protector with integral 13 dB switchable attenuator for dynamic range extension has been developed which overcomes the limitations of previously developed circuits. High power is handled by using a unique multistage multiple diode circuit to reduce the diodes' thermal resistance. Low loss and good match with constant values of attenuation is achieved by using broadband circuit techniques to be described.

This receiver protector (RP) proceeds the LNA for typical applications. A circulator with a terminated load could be used preceding the RP to provide a matched system in the high input power state with the load of the circulator dissipating the RP's reflected power. Another system application would be to have a two channel system with an input 3-dB Lange coupler, cascaded with two RPs on the coupler outputs, two LNAs, and an output 3-dB Lange coupler. This arrangement provides a well matched receiver for all input power levels, with the load of the input Lange coupler dissipating the receiver protectors reflected power. This configuration provides for a 3-dB increase in the overall third order intercept point and input power handling capability over a single channel system.

MMIC CIRCUIT AND LAYOUT

The MMICs were designed by the authors listed in this paper and were fabricated at the Texas Instruments foundry using their design rules. The MMIC circuit was constructed on 150 micron thick semi-insulating GaAs for low

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loss. There was a minor difference in the diode's thermal resistance between 100 and 150 micron thick GaAs since the diodes act as point sources on top of the substrate. Figure 1 illustrates the schematic of the first implementation of the RP/Attenuator (Circuit A). Eight PIN limiter diodes are coupled to the main transmission line in shunt to ground. Each PIN diode has an I region thickness of 1.2 microns (the standard Texas Instruments PIN) with a larger than normal diameter of 0.8 microns for high power handling capacity. The PIN diodes on resistance is about 2.5 ohms with an off capacitance of 0.035 pF. Each of the 4 attenuator diodes have diameter of 0.6 microns, an on resistance of 2.5 ohms and an off capacitance of 0.022 pF.

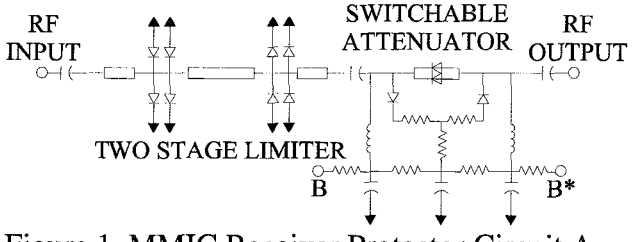

Figure 1. MMIC Receiver Protector Circuit A

The first cluster of four diodes located at the RF input reflects the incident RF, and the second cluster provides additional isolation to the output. The diodes are arranged back to back to provide an internal path for the DC rectified current. This circuit provides extremely fast turn on and fast recovery time without the need for external bias. The use of four diodes in parallel greatly reduces the temperature rise of the diode compared to the use of a single diode of the equivalent area. The limiter three interconnecting transmission lines are of a higher characteristic impedance than 50-ohm providing a series inductance which was found to match the diodes over a 2:1 bandwidth. The second cluster of diodes is separated from the first cluster optimally to provide the highest isolation for the diode combination.

The attenuator consists of a matched tee pad which is coupled to or decoupled from the circuit by use of four PIN diodes with the associated dual rail TTL input voltage B - B*. The three tee pad resistor values are selected for the required attenuator value and good match. The main transmission line contains two parallel connected diodes in series with the main line to reduce the low loss state attenuation. All capacitors are similar and are used for RF bypassing or dc blocking. The resistors on each side of the bottom of the tee attenuator provide a diode dc path should both shunt attenuator diodes fail to open at the same time, assuring good recovery time. The bias is injected into the attenuator circuit with shunt bypass capacitors and with series spiral inductors which are suspended above the circuit using air bridge technology to provide high inductance, low circuit loss, and good VSWR over octave bandwidth. This attenuator is robust in that it is relatively insensitive to parameter changes like sheet resistivity of the tee pad TaN resistive material used for the resistors.

Figure 2 illustrates another implementation of the circuit (circuit B). This circuit is similar to the previous circuit except for the way the PIN limiter diodes are coupled. In this circuit, the input diode pairs are series dc coupled to the output diode pairs through connecting lines The limiter diodes are grounded at RF by way of bypass capacitors instead of via holes as with the circuit A. This circuit provides lower leakage compared to circuit A since the input limiter diodes provide a current drive for the second stage diodes by way of the common dc path. This provides similar attenuation in the first and second stage of the limiter even though the I regions of all diodes are similar. In circuit A, the input diodes provide more attenuation compared to the output stage except at complete saturation. The power handling capability of circuit B is about 3 dB lower than that of circuit A.

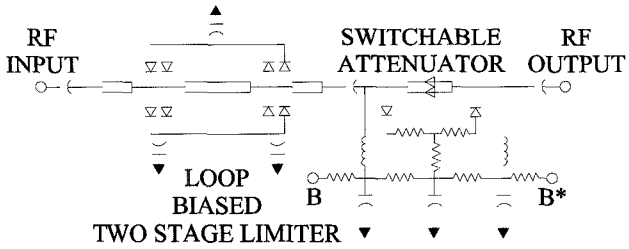

Figure 2. MMIC Receiver Protector Circuit B

Figure 3 illustrates the MMIC layout of circuit A with two identical circuits for a balanced two-channel system. The circuit is optimized for low loss and good VSWR with all bias circuits and DC blocking incorporated on the circuit. The diodes are isolated thermally, to take advantage of the thermal resistance lowering using multiple diodes. The three high impedance matching lines of the limiter are chosen to provide excellent broadband match and low VSWR over an octave bandwidth.

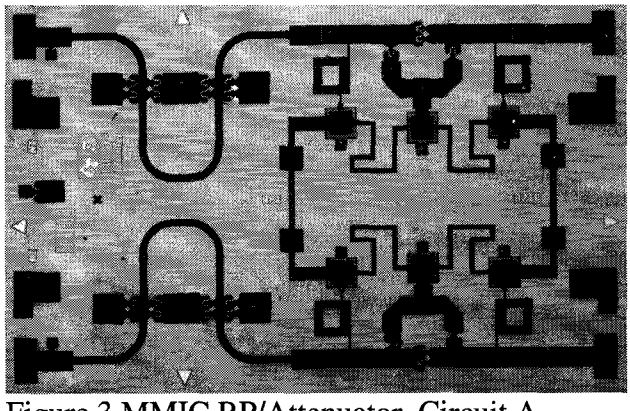
Figure 3 MMIC RP/Attenuator, Circuit A

The attenuator layout also is arranged to have the tee pad completely out of the circuit in the low loss state. The attenuator is matched in both states considering the diode parasitic elements, series PIN on inductance, and shunt off capacitance. In the attenuator low loss state the additional shunting capacitance of shunt diodes and their short pads to the main line is compensated by the series inductance of the series diodes for low loss and low VSWR. With the attenuator activated, the shunting effect of the open diodes and their pads is compensated by the series inductance of the on diodes. In the attenuator, the width of the resistors match the transmission line width for good frequency response and constant attenuation .

Figure 4 illustrates the second embodiment of the circuit with the diode pairs connected by dc transmission lines with two identical circuits for a balanced two channel system. The diodes are RF shorted to ground with bypass capacitors. The rest of the circuit is similar to circuit A.

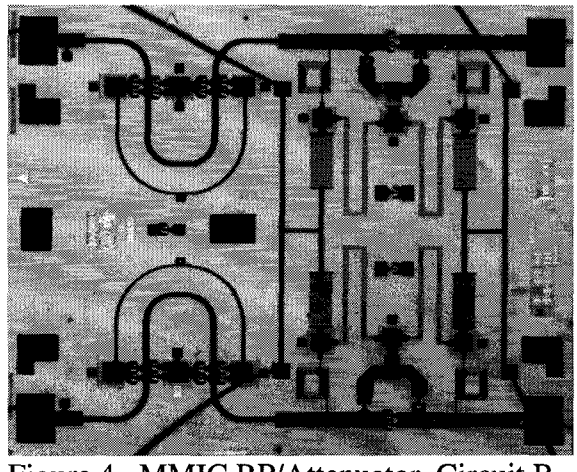
Figure 4. MMIC RP/Attenuator, Circuit B

EXPERIMENTAL RESULTS

The circuits were fabricated and evaluated with the following results:

Bandwidth:	Octave, - X band
Insertion loss:	0.55 to 0.70 dB
Return loss:	15 to 30 dB
Recovery time:	50 ns
Third order input intercept point:	28 dBm
13 dB attenuator value:	12.8 ± 0.5 dB
Attenuator on switching time:	10 ns
Attenuator off switching time	50 ns
Flat leakage level:	50 mW

Spike leakage level: 100 mW

Figure 5 illustrates the measured input-output power for the two circuits under CW operation. Circuit B has a reduced leakage power compared to circuit A because the input diodes turn on the second stage diodes providing lower leakage levels. It was found that circuit A had about 3 dB more power handling capability than circuit B. The power handling capability depends on the pulse width and the duty cycle. Circuit A can handle about 2 watts CW and significantly higher power levels for pulsed operation.

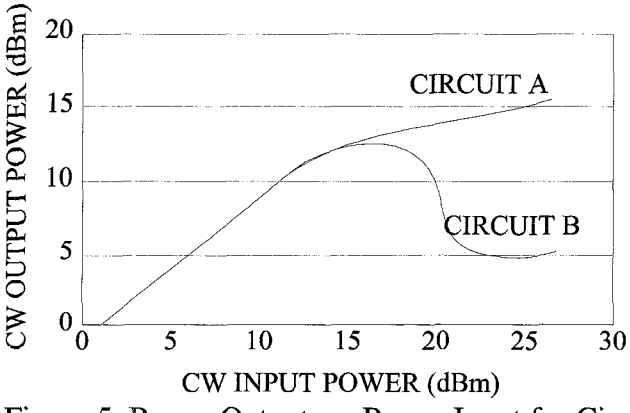

Figure 5. Power Output vs. Power Input for Circuits A and B under CW operation

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CONCLUSION

A unique receiver protector/attenuator has been developed that provides state-of-the-art performance in a robust, low cost, MMIC.

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